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OFFSET TRIM CIRCUIT AND METHOD FOR A CONSTANT-TRANSCONDUCTANCE RAIL-TO-RAIL CMOS INPUT CIRCUIT

Field of the Invention

The present invention is related to offset trimming, and, in particular, to a system and method for a rail-to-rail CMOS input circuit with constant transconductance and offset trimming.

Background of the Invention

Rail-to-rail input stages are important for low-supply voltage systems which are used in many system applications. A well-known problem of rail-to-rail input stages is offset glitch. Most rail-to-rail input stages include a p-type differential pair and an n-type differential pair. For this configuration, the p-type differential pair is active only for low input common mode voltages, and the n-type differential pair is only active for high input common mode voltages. However, the input offset voltage must make a transition between the offset of the p-type differential pair to the n-type differential pair when the input common mode voltage increases from low to high values. The transition often causes rail-to-rail MOS operational amplifiers to have a poor common mode rejection ratio (CMRR).

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention as described with reference to the following drawings.

FIG. 1 illustrates a block diagram of a circuit; and

FIG. 2 shows a schematic diagram of an input circuit that is arranged in accordance with aspects of the present invention.

Detailed Description of a Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and

assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to a constant-transconductance rail-to-rail CMOS input circuit with offset trim. PMOS and NMOS differential trim stages are scaled versions of PMOS and NMOS input stages respectively. The differential trim stages are configured to adjust the offset of the differential output current with accuracy over temperature. A first current mirror circuit is configured to receive a fraction of a bias current (βI), where β is related to the input common mode voltage. A second current mirror circuit is configured to receive another fraction of the bias current ($(1-\beta)I$). The first current mirror circuit is configured to provide current βI to the PMOS input stage, and a scaled-down version of current βI to the PMOS differential trim stage. The second current mirror circuit is configured to provide current ($(1-\beta)I$) to the NMOS input stage, and a scaled-down version of current ($(1-\beta)I$) to the differential PMOS trim stage.

FIG. 1 is illustrates a block diagram of a circuit (100) that includes input circuit 102 and summer circuit 104. Input circuit 102 is a CMOS input circuit that is configured for rail-to-rail operation. Input circuit 102 is arranged to trim the offset with accuracy

over temperature, and further arranged to have a relatively constant transconductance over a range of input common mode voltage. Input circuit 102 is configured to receive a differential input signal (V_{in}=inP-inM), a differential PMOS trim signal ($V_{trim,p}$=PtrimP-PtrimM), and a differential NMOS trim signal ($V_{trim,n}$=NtrimP-NtrimM). Input circuit 102 is further configured to provide a PMOS differential output current (out_high_P-out_high_M) and an NMOS differential output current (out_low_P-out_low_M) in response to the differential input signal.

Summer circuit 104 is configured to provide a differential output current (I_{out}=IP-IM) in response to the PMOS differential output current and the NMOS differential output current. The differential output current is the sum of the PMOS differential output current and the NMOS differential output current. An exemplary summer circuit 104 could include a folded cascode circuit.

FIG. 2 is an illustration of a schematic diagram of an input circuit (102). Transistors M1 and M2 are PMOS devices that are arranged to operate as a differential pair that receives tail current I1. Transistors M1 and M2 are driven by the differential input signal (inP-inM). Transistors M11 and M12 are scaled versions (e.g., scaled by a factor α) of transistors M1 and M2 that receive tail current I2. Transistors M11 and M12 are configured to receive the differential PMOS trim signal (PtrimP-PtrimM) on the gates of transistors M11 and M12. Transistors M1 and M2 are arranged to operate as a PMOS input stage. Transistors M11 and M12 are configured to operate as a PMOS trim stage.

Transistors M3 and M4 are NMOS devices that are configured to operate as a differential pair that receives tail current I3. Transistors M13 and M14 are scaled versions (e.g., scaled by a factor α) of transistors M3 and M4 that receive tail current I4. Transistors M13 and M14 are configured to receive the differential NMOS trim signal (NtrimP-NtrimM) on the gates of transistors M13 and M14. Transistors M3 and M4 are arranged to operate as an NMOS input stage. Transistors M13 and M14 are configured to operate as an NMOS trim stage.

The input common mode voltage is detected on the sources of transistors M1 and M2. The input common mode voltage is also detected on the gate of transistor M8. Transistor M19 is configured to operate as a bias current source that provides a bias current (I5) to the source of transistors M7 and M8. Transistors M7 and M8 are arranged

to operate as a current switch that compares the input common mode voltage (detected at the sources of transistors M3 and M4) to a reference voltage at the gate of transistor M7.

At high input common mode voltages, transistor M8 is off and transistor M7 conducts. Transistors M9, M16, and M6 are configured to operate as a current mirror. Bias current I5 is mirrored through transistor M9 to transistor M6 to provide tail current I3, and to transistor M16 to provide tail current I4. Transistors M16 and M6 are ratioed such that tail current I4 is a scaled-down version of tail current I3 (e.g., scaled by factor α). At high input common mode voltages, approximately no current is flowing into transistor M10, and therefore tails current I1 and I2 are approximately zero.

At low input common mode voltages, transistor M7 is off and transistor M8 conducts. Approximately all of the bias current (I5) flows through transistor M10. Transistors M10 and M17 are arranged to operate as a current mirror. Current I5 is reflected to provide current I6. Transistors M30, M15, and M5 are arranged to provide another current mirror. Current I6 is reflected to provide tail currents I1 and I2. Transistors M15 and M5 are ratioed such that tail current I2 is a scaled down version of tail current I1 (e.g., scaled by factor α). At low input common mode voltages, there is approximately no current is flowing into transistor M9, and therefore tails current I3 and I4 are approximately zero. At input common mode voltages close to the reference voltage (Vref), bias current I5 is gradually moved from one of the two input stages to the other. The transition is more gradual when the transconductance of transistors M7 and M8 are low. The transconductance of transistors M7 and M8 can be made low, for example, by using long, narrow devices for transistors M7 and M8.

Transistors M20-M29 are each configured to operate as a cascode transistor.

Transistors M1-M4 are all biased to operate in subthreshold (i.e. $V_{GS}<V_{th}$). In subthreshold, the drain current of a MOSFET is given by: $I_d=I_{d0}\exp((V_{GS}-V_{th})/(n * V_t))$, where n is the subthreshold slope factor. I_{d0} is proportional to W/L. A threshold voltage mismatch ΔVth between the NMOS input stage and the PMOS input stage causes an input voltage offset of equal magnitude. Accordingly, the input referred offset (Vos) of a MOS input stage is given by $Vos= \Delta V_{th} + nV_t * (\Delta I_{d0}/I_{d0})$. This equation includes only the contribution of the input MOSFETs themselves. This equation includes one temperature-dependent term and one temperature-independent term. The NMOS and

PMOS input stages can be designed such that the term ΔV_{th} dominates. Since ΔVth is temperature-independent, the offset trim can be made relatively accurate over the operating range of the circuit using a temperature-independent trim when the transistors of the NMOS and PMOS input stages are biased in subthreshold.

At input common mode voltages close to Vref, if the current mirrors have a one-to-one ratio, a fraction β of the bias current (I5) flows through the NMOS input stage and another fraction $(1-\beta)$ of the bias current flows through the PMOS input stage. According to one example, the current mirror formed by transistors M6 and M9 and the current mirror formed by transistors M5 and M30 each have a scaling ratio of k. In this example, $I1 = k * \beta * I5$ and $I3 = k * (1-\beta) * I5$. The differential output current (I_{out}) is given by $I_{out} = V_{in} * (g_{m,n} + g_{m,p})$, where Vin is the differential input voltage (inP-inM), $g_{m,n}$ is the transconductance of the NMOS input stage, and $g_{m,p}$ is the transconductance of the PMOS input stage. Substituting the subthreshold value of g_m into this equation gives $I_{out} = (V_{in} * k * \beta * I5)/(nV_t) + (V_{in} * k * (1-\beta) * I5)/(nV_t) = (V_{in} * k * I5)/(n V_t)$, where it is assumed that the subthreshold slope (n) for the NMOS and PMOS devices is the same. This equation shows that the transconductance of the input stage is the same across the entire input common mode voltage range. If the subthreshold slopes are not the same for the p-channel and n-channel devices, there may be a slight variation in the transconductance across the input common mode voltage range.

The differential output current due to offset (I_{os}) is given by: $I_{os} = (V_{os,n} * k * \beta * I5)/(nV_t) + (V_{os,p} * k * (1-\beta) * I5)/(nV_t)$, wherein $V_{os,n}$ and $V_{os,p}$ are the threshold voltage mismatch of the NMOS input stage and the PMOS input stage respectively. The differential output current due to the differential trim stage (Itrim) is given by: $Itrim = (V_{trim,n} * k * \beta * I5)/(\alpha nV_t) + (V_{trim,p} * k * (1-\beta) * I5)/(\alpha nV_t)$, where $\alpha = g_{m,in}/g_{m,trim}$, and $g_{m,trim}$ is the transconductance of the differential trim stage. The ratio between $g_{m,in}$ and $g_{m,trim}$ is equal to α because of the transistor and tail current scaling. Accordingly, the offset is cancelled for all input common mode voltages when $V_{trim,n} = \alpha V_{os,n}$ and $V_{trim,p} = \alpha V_{os,p}$.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention,

the invention also resides in the claims hereinafter appended and legal equivalents. Any element in a claim that does not explicitly use the phrase "means for" or "step for" is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. § 112, paragraph 6.